DATA SHEET

ISS
I2C remote control Sound System

Product specification

2002 Apr 13

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

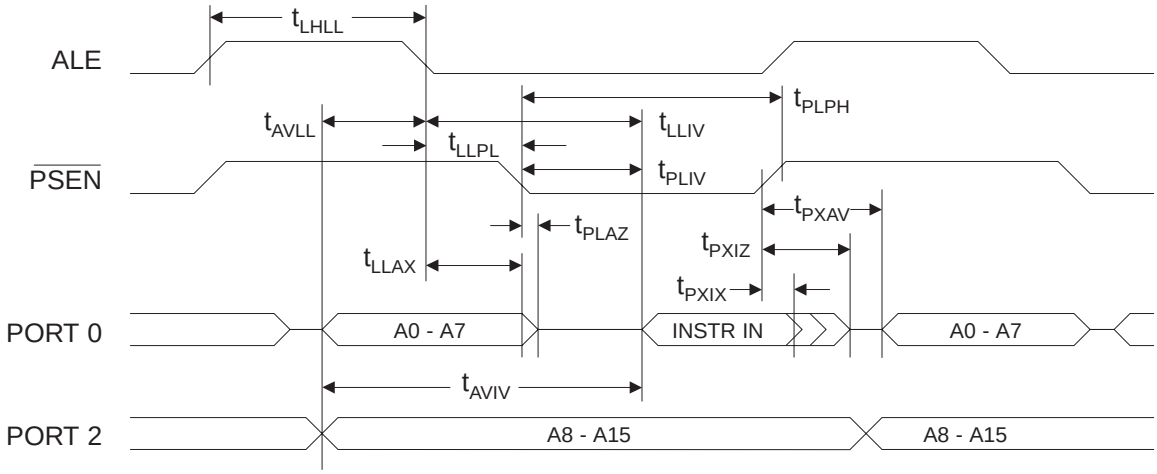
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

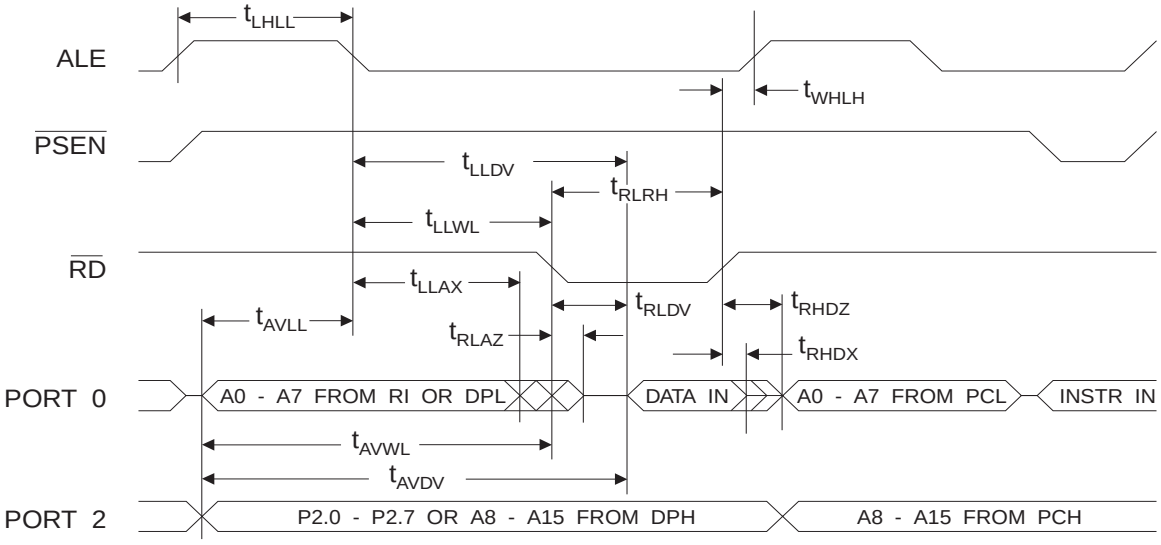
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

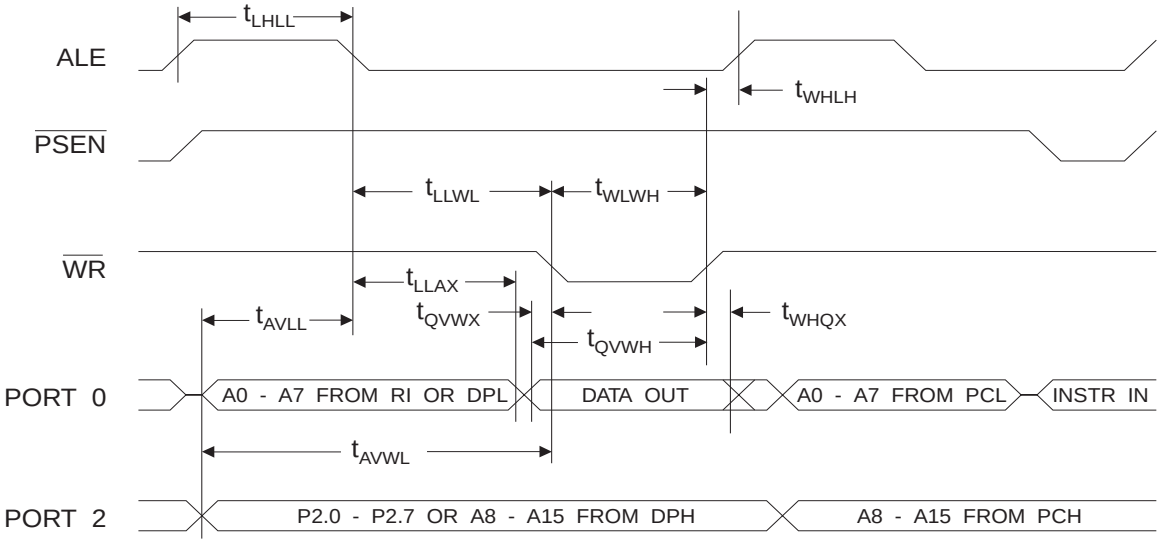
External Program Memory Read Cycle



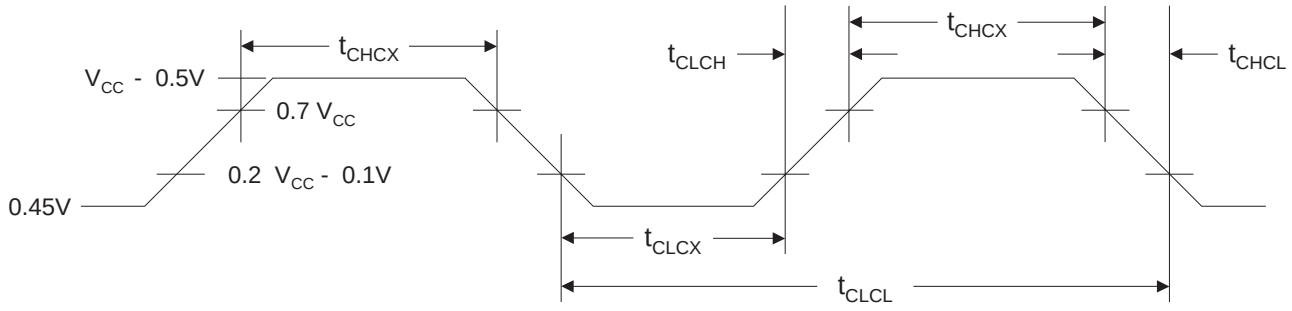
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms

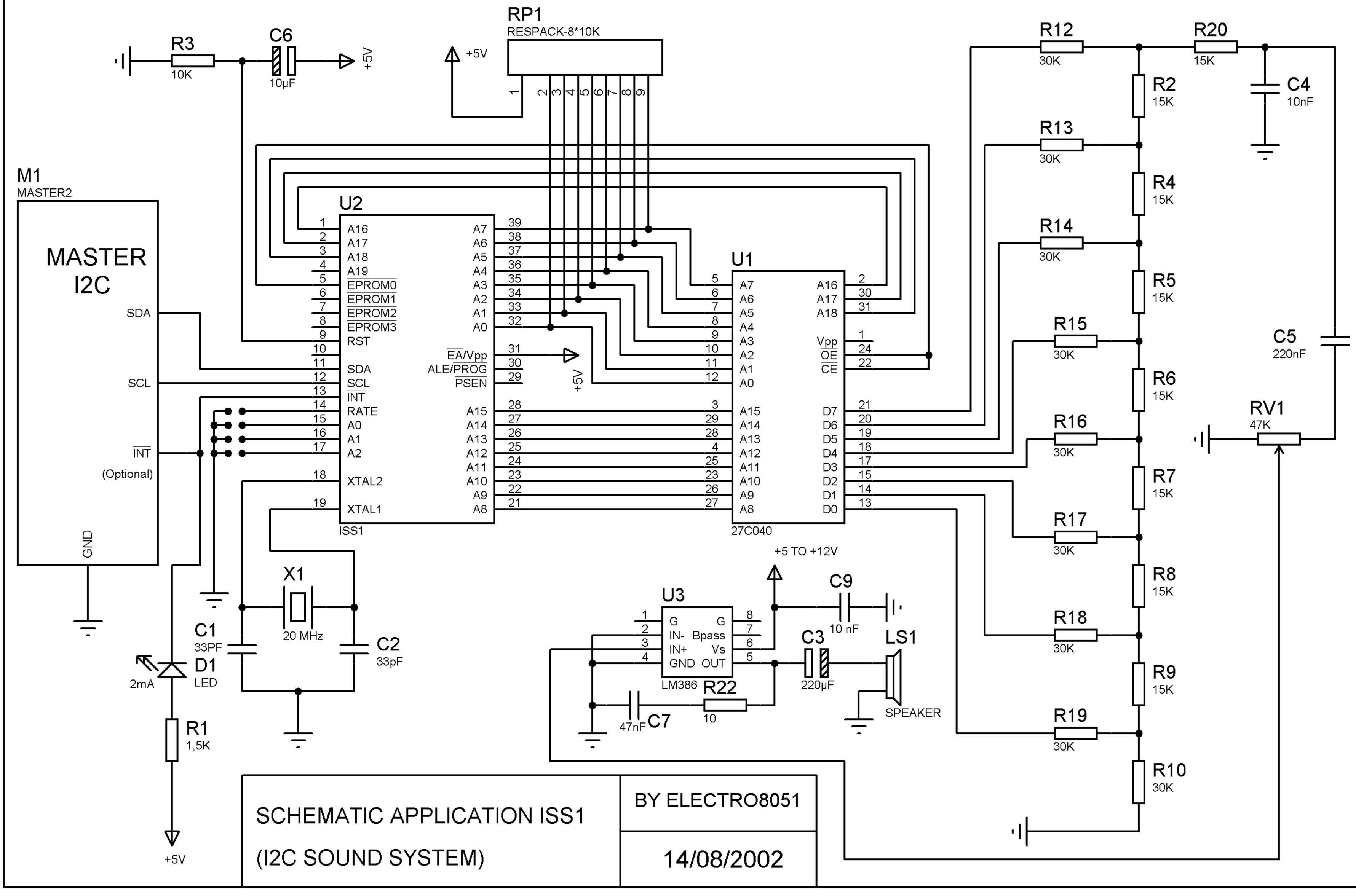


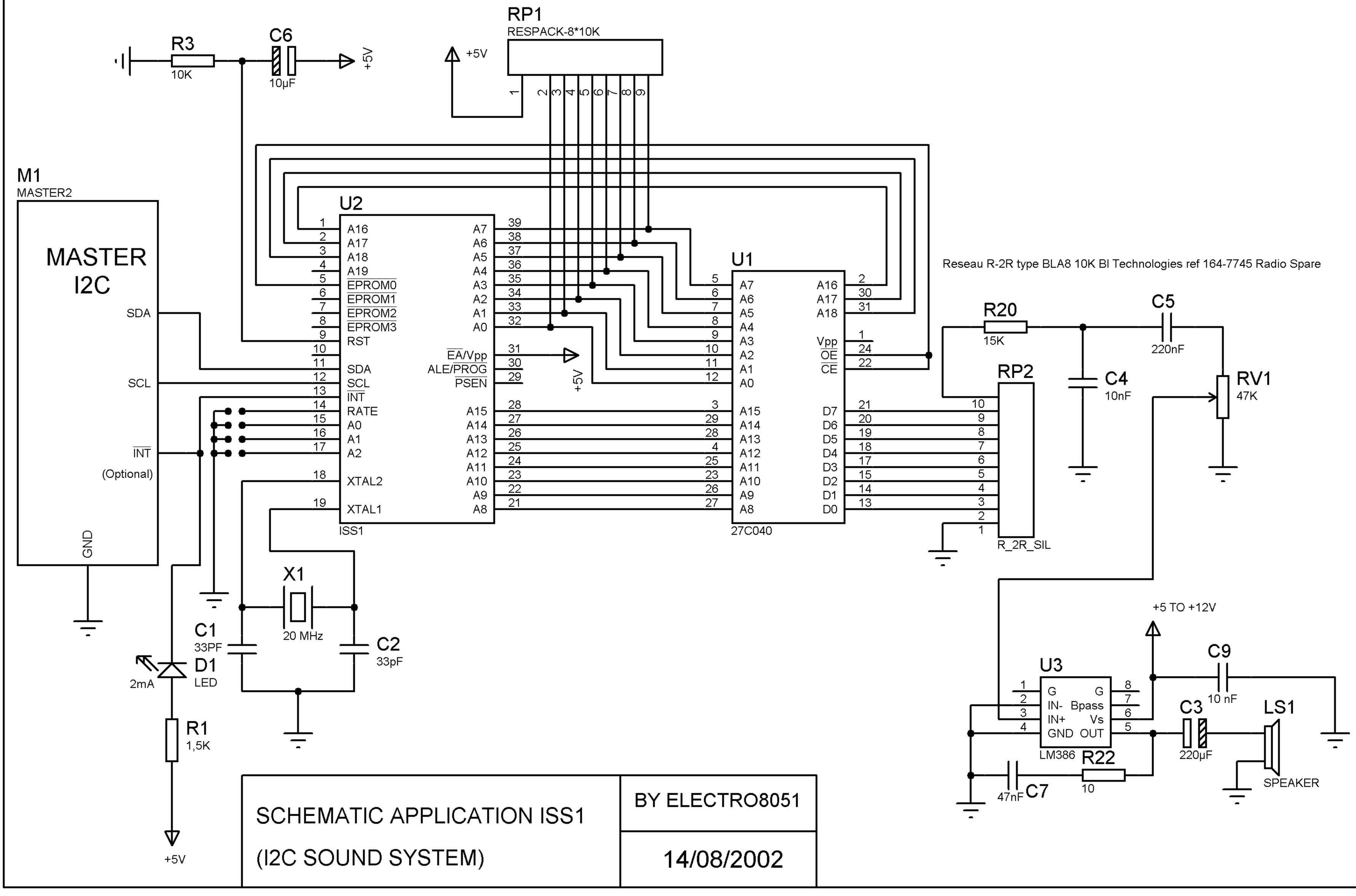
External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

ISS DIP 40 package

Pin	Name	Type	Active	Use
1	A16	Output	High	Address bit 16
2	A17	Output	High	Address bit 17
3	A18	Output	High	Address bit 18
4	A19	Output	High	Address bit 19
5	EPROM0	Output	Low	Select eprom 0
6	EPROM1	Output	Low	Select eprom 1
7	EPROM2	Output	Low	Select eprom 2
8	EPROM3	Output	Low	Select eprom 3
9	RST	Input	High	Reset
10	Reserved			
11	SDA	Input/output	Low	I2C SDATA
12	SCL	Input/output	Low/High	I2C SCLOCK
13	INT	Output	Low	Interrupt(low when ISS buzy)
14	RATE	Input	Must be tired to 0V or VCC	Low=8Khz,High=11,025Khz
15	A0	Input	Must be tired to 0V or VCC	
16	A1	Input	Must be tired to 0V or VCC	
17	A2	Input	Must be tired 0V or VCC	
18	XTAL2	Input	To crystal 16 mhz	
19	XTAL1	Input	To crystal 16 mhz	
20	Ground	Power		
21	D0	LSB output	High	To D/A converter
22	D1	D1 output	High	To D/A converter
23	D2	D2 output	High	To D/A converter
24	D3	D3 output	High	To D/A converter
25	D4	D4 output	High	To D/A converter
26	D5	D5 output	High	To D/A converter
27	D6	D6 output	High	To D/A converter
28	D7	MSB output	High	To D/A converter
29	PSEN	Output	Low	Unused
30	ALE	Output	High	Unused
31	EA	Input	Must be tired to VCC	
32	A0	Output	Address A0	To Eprom(s)
33	A1	Output	Address A1	To Eprom(s)
34	A2	Output	Address A2	To Eprom(s)
35	A3	Output	Address A3	To Eprom(s)
36	A4	Output	Address A4	To Eprom(s)
37	A5	Output	Address A5	To Eprom(s)
38	A6	Output	Address A6	To Eprom(s)
39	A7	Output	Address A7	To Eprom(s)
40	VCC	Power		


R3
10K
C6
10µF
+5V
RP1
RESPACK-8*10K
M1
MASTER2
MASTER
I2C
SDA
SCL
INT
(Optional)
GND
U2
A16
A17
A18
A19
EPROM0
EPROM1
EPROM2
EPROM3
RST
SDA
SCL
INT
RATE
A0
A1
A2
XTAL2
XTAL1
A7
A6
A5
A4
A3
A2
A1
A0
EA/Vpp
ALE/PROG
PSEN
A15
A14
A13
A12
A11
A10
A9
A8
ISS1
U1
A7
A6
A5
A4
A3
A2
A1
A0
A15
A14
A13
A12
A11
A10
A9
A8
A16
A17
A18
Vpp
OE
CE
D7
D6
D5
D4
D3
D2
D1
D0
27C040
X1
20 MHz
C1
33PF
C2
33pF
D1
LED
2mA
R1
1,5K
+5V
+5 TO +12V
U3
G
G
IN-
Bpass
IN+
Vs
GND
OUT
LM386
C9
10 nF
C3
220µF
LS1
SPEAKER
R22
10
C7
47nF
R12
30K
R20
15K
C4
10nF
R2
15K
R13
30K
R4
15K
R14
30K
R5
15K
R15
30K
C5
220nF
R6
15K
RV1
47K
R16
30K
R7
15K
R17
30K
R8
15K
R18
30K
R9
15K
R19
30K
R10
30K
SCHEMATIC APPLICATION ISS1
(I2C SOUND SYSTEM)
BY ELECTRO8051
14/08/2002


R3
10K
C6
10µF
+5V
RP1
RESPACK-8*10K
+5V
M1
MASTER2
MASTER
I2C
SDA
SCL
INT
(Optional)
GND
U2
A16
A17
A18
A19
EPROM0
EPROM1
EPROM2
EPROM3
RST
SDA
SCL
INT
RATE
A0
A1
A2
XTAL2
XTAL1
A7
A6
A5
A4
A3
A2
A1
A0
EA/Vpp
ALE/PROG
PSEN
A15
A14
A13
A12
A11
A10
A9
A8
ISS1
U1
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OE
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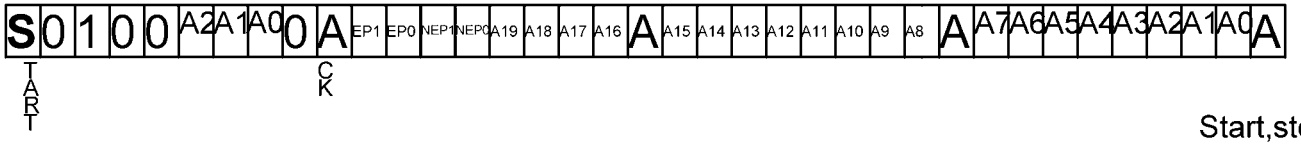
D7
D6
D5
D4
D3
D2
D1
D0
27C040
Reseau R-2R type BLA8 10K BI Technologies ref 164-7745 Radio Spare
R20
15K
C5
220nF
RP2
C4
10nF
RV1
47K
R_2R_SIL
X1
20 MHz
C1
33PF
C2
33pF
D1
LED
2mA
R1
1,5K
+5V
+5 TO +12V
U3
G
G
IN-
Bpass
IN+
Vs
GND
OUT
LM386
C9
10 nF
C3
220µF
LS1
SPEAKER
R22
10
C7
47nF
SCHEMATIC APPLICATION ISS1
(I2C SOUND SYSTEM)
BY ELECTRO8051
14/08/2002

WRITE I2C TO ISS1

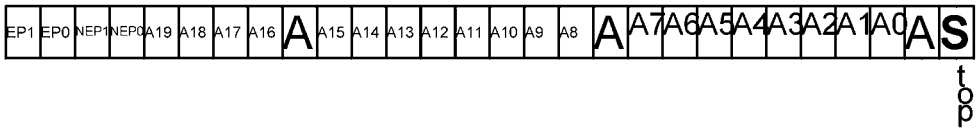
Slave adress

START ADRESS



Start,stop,data :send by master
Synchro : send by master
Ack : send by ISS1

END ADRESS



EPROM	EP1	EP0	Start adress	End adress
27C512	0	0	00000	0FFFF
27C1001	0	1	00000	1FFFF
27C010	0	1	00000	1FFFF
27C040	1	0	00000	7FFFF
27C080	1	1	00000	FFFFF

N° of eprom	NEP1	NEP0
Eprom n°1	0	0
Eprom n°2	0	1
Eprom n°3	1	0
Eprom n°4	1	1

EPROM	KO	RATE=1 8khz	RATE=0 11,025khz	EP1	EP0
27C512	64	7,8125s	5,66s	0	0
27C1001	128	15,625s	11,338s	0	1
27C010	128	15,625s	11,338s	0	1
27C040	512	62,5s	45,35s	1	0
27C080	1024	125s	90,7s	1	1

EP1,EP0 must be the same in Start and end adress

NEP1,NEP0 in end adress >= NEP1,NEP0 instart adress

Eproms must be identical,4 eproms max

Example

The ISS is used with 2 Eproms 27C040 and the message to be send begin on first eprom at address 50000H and end on second eprom at address 3FFFFH.

A2,A1,A0 are tired to 0V.

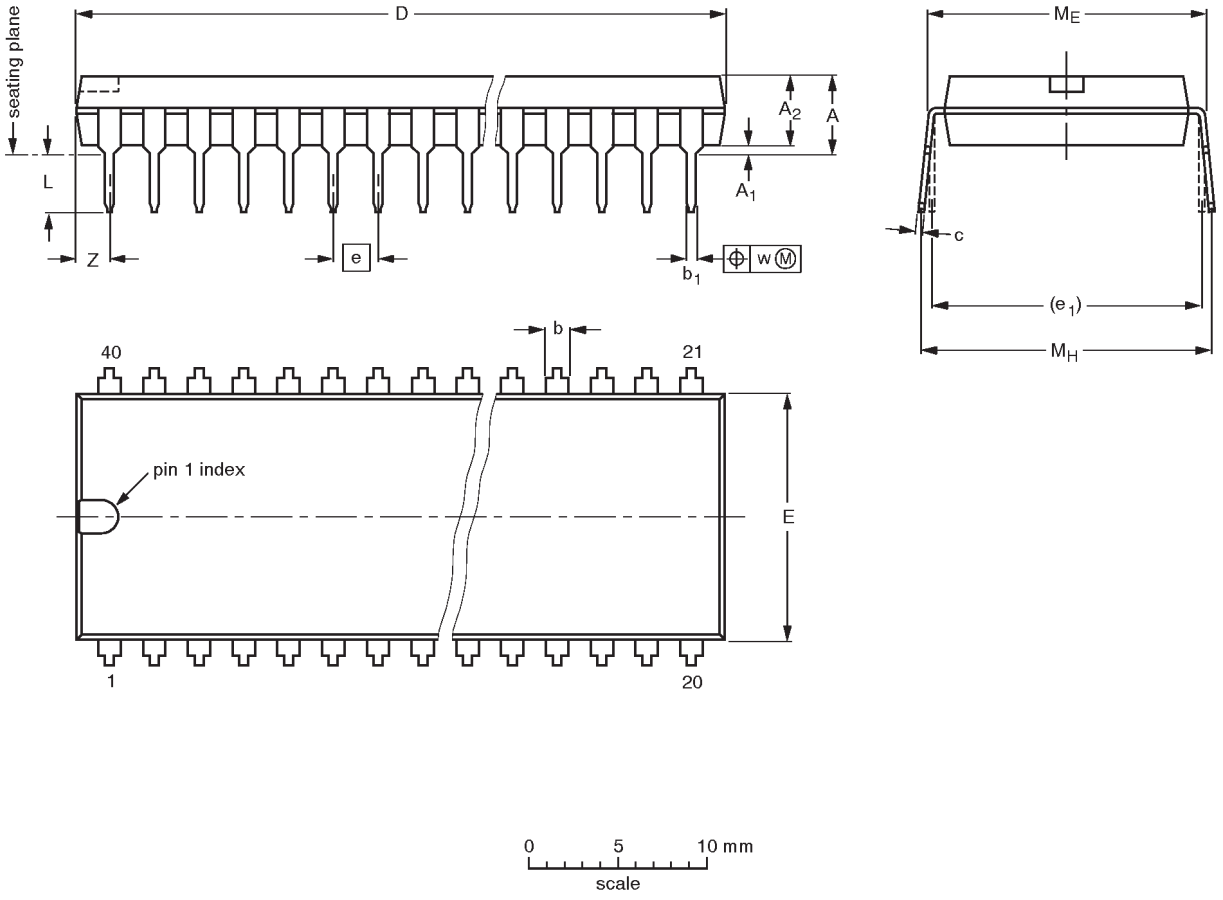
The master has to send :

Slave address : 40H

Start address : 85H 00 00 EP1,EP0= 1,0 (27C040) NEP1,NEP0=0,0 (1°Eprom)

End address : 93H FFH FFH EP1,EP0=1,0 (27C040) NEP1,NEP0=0,1 (2° Eprom)

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14